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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500.00

Complete if Known	
Application Number	10/657,181-Conf. #1619
Filing Date	September 9, 2003
First Named Inventor	Chun-Lung CHIU
Examiner Name	A. T. Luu
Art Unit	2816
Attorney Docket No.	2519-0122PUS1

METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☐ Deposit Account Deposit Account Number: 02-2448 Deposit Account Name: Birch, Stewart, Kolasch & Birch, LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - =	_____ x	_____ =	

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - =	_____ x	_____ =	

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims

Fee ($)	Fee Paid ($)

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ /50	_____ (round up to a whole number) x	_____ =	

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal	500.00

SUBMITTED BY

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TRANSMITTAL OF APPEAL BRIEF

Docket No.
2519-0122PUS1

In re Application of: Chun-Lung CHIU et al.

Application No.	Filing Date	Examiner	Group Art Unit
10/657,181-Conf. #1619	September 9, 2003	A. T. Luu	2816

Invention: PWM BUFFER CIRCUIT FOR ADJUSTING A FREQUENCY AND A DUTY CYCLE OF A PWM SIGNAL

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: September 5, 2006 .

The fee for filing this Appeal Brief is $ 500.00 .

[x] Large Entity [ ] Small Entity

[ ] A petition for extension of time is also enclosed.

The fee for the extension of time is _____ .

[x] A check in the amount of $ 500.00 is enclosed.

[ ] Charge the amount of the fee to Deposit Account No. 02-2448 .
This sheet is submitted in duplicate.

[ ] Payment by credit card. Form PTO-2038 is attached.

[x] The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. 02-2448 .
This sheet is submitted in duplicate.

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Dated: November 3, 2006

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Docket No.: 2519-0122PUS1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Chun-Lung CHIU et al.

Application No.: 10/657,181 | Confirmation No.: 1619

Filed: September 9, 2003 | Art Unit: 2816

For: PWM BUFFER CIRCUIT FOR ADJUSTING A FREQUENCY AND A DUTY CYCLE OF A PWM SIGNAL | Examiner: A. T. Luu

APPELLANT'S BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 3, 2006

Sir:

This brief is filed within two months of the Notice of Appeal filed in this case on September 5, 2006.

The fees required under § 1.17(f) and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Invention
VI.	Issues
VII.	Grouping of Claims

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Delta Electronics Inc., as recorded in an assignment at reel 014477, frame 0964, recorded September 9, 2003.

II. RELATED APPEALS, INTERFERENCES AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 19 claims pending in the application.

B. Current Status of Claims

1. Claims cancelled: 8 and 18

2. Claims withdrawn from consideration but not canceled: None

3. Claims pending: 1-7, 9-17, 19-21

4. Claims allowed: None

5. Claims rejected: 1, 3, 4, 6, 7, 9-11, 13, 14, 16, 17 and 19-21

6. Claims Objected to but indicated as being allowable if rewritten in independent form: 2, 5, 12 and 15

C. Claims On Appeal

The claims on appeal are claims 1, 3, 4, 6, 7, 9-11, 13, 14, 16, 17 and 19-21

IV. STATUS OF AMENDMENTS

A Response was filed on July 5, 2006, but did not include any amendments. The Advisory Action of August 2, 2006, indicated that the Request for Reconsideration do not place the application in condition for allowance because the argument was not persuasive. Applicants also filed a Pre-Appeal Brief Request for Review on September 5, 2006. A Notice of Panel Decision dated September 26, 2006, indicated that the application remains under appeal because there is at least one actual issue for appeal.

V. SUMMARY OF INVENTION

In general, the present invention relates to a control circuit for the speed of a fan motor. As shown in Figure 2 and described in paragraph 0011, lines 4-8, a PWM signal generation unit 10 provides a first signal S1 to a PWM buffer circuit 20 which converts the first signal to second signal S2 which is input to driving circuit 11 which drives fan motor 12. As shown in Figure 3 and described at paragraph 0014, lines 2-4 and paragraph 0016, line 5, the buffer circuit 20

includes a duty cycle converting circuit 21 and a frequency-fixed PWM signal generating circuit 22. The signal generating circuit 22 includes a frequency controller 23 and a PWM signal generator 24. Figure 5 shows the detailed circuitry of elements 21, 22, 23 and 24. This is described in paragraphs 0017-0020.

Independent Claim 1

Claim 1 describes the buffer circuit 20 (Figure 2, paragraph 0014, lines 2-4) as including a duty cycle converting circuit 21 (Figure 3) for receiving first signal S1 (paragraph 0014, line 5) and generating a duty cycle reference voltage V1 (paragraph 0014, line 5). The buffer also includes a frequency-fixed PWM signal generating circuit (22) for outputting a second signal S2 (paragraph 0014, line 9).

Claim 2

Claim 2 describes the detailed circuitry of the duty cycle converting circuit 21 as shown in Figure 5 and described in paragraph 0017, including transistor Q1, resistors R1 to R5, diode D1, capacitors C1 and operational amplifier OA1.

Claim 3

Claim 3 describes the embodiment where the frequency-fixed PWM signal generating circuit 22 is implemented by a microchip control unit. This is shown as element 30 in Figure 6 and described in paragraph 0016.

Claim 4

Claim 4 describes the signal generating circuit 22 as including a frequency controller 23 and a PWM signal generator 24, shown in Figure 3 and described in paragraph 0016, line 5.

Claim 5

Claim 5 describes the details of the frequency controller 23, shown in Figure 5 and described in paragraph 0019 as including the operational amplifier OA2, three resistors R6-R8 and a capacitor C2.

Claim 6

Claim 6 describes the details of PWM signal generator 24 shown in Figure 5 and described in paragraph 0020 as including operational amplifier OA3 and resistor 9.

Claim 7

Claim 7 describes the frequency control signal FC shown in Figure 5 and described in paragraph 0019, lines 10-12 as a continuous triangular wave signal.

Claim 9

Claim 9 recites the frequency of the second signal and the frequency and duty cycle of the first signal as described in paragraph 0013.

Independent Claim 10

Claim 10 describes a control circuit including a PWM signal generation unit 10, a PWM buffer circuit 20 and a driving circuit 11 shown in Figure 2 and described in paragraph 0011, line 4.

Claim 11

Claim 11 includes the same limitations as claim 1.

Claim 12

Claim 12 contains the same limitations as claim 2.

Claim 13

Claim 13 includes the same limitations as claim 3.

Claim 14

Claim 14 includes the same limitations as claim 4.

Claim 15

Claim 15 includes the same limitations as claim 5.

Claim 16

Claim 16 includes the same limitations as claim 6.

Claim 17

Claim 17 includes the same limitations as claim 7.

Claim 19

Claim 19 includes the same limitations as claim 9.

Independent Claim 20

Claim 20 includes the limitations found in a combination of claims 1 and 3 and accordingly the descriptions provided in those two claims above also apply here.

Independent Claim 21

Claim 21 includes the limitations of claims 10, 11 and 13. Accordingly, the descriptions in those three claims above also apply here.

VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 4, 7 and 9 were rejected under 35 U.S.C. 102(b) as being anticipated by Seong (US Patent 5,606,296).

2. Claims 3 and 20 were rejected under 35 U.S.C. 103(a) as being obvious over Seong.

3. Claims 6, 10, 11, 13, 14, 16, 17, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seong in view of Hoffman (US Patent 5,457,435).

VII. ARGUMENT

Rejection of Claims 1, 4, 7 and 9 Under 35 U.S.C. 102(b) as being anticipated by Seong (US Patent 5,606,296).

The Examiner states that Figure 3 of the reference includes a duty cycle converting circuit 301 for receiving a first PWM signal Vo and generating a duty cycle reference voltage Vcon based on the first signal and a frequency-fixed PWM signal generating circuit which includes the rest of the circuit shown in Figure 3 for receiving the reference voltage and outputting a second PWM signal having a fixed-frequency.

Independent Claim 1

Applicants disagree with the Examiner's understanding of the Seong reference. Specifically, Applicant's submit that even if the circuits labeled 100, 200 and 302 in figure 3 of the reference show a signal generating circuit, that is not a frequency-fixed PWM signal generating circuit and it does not output a second PWM signal at a fixed frequency. Applicants

submit that this part of the Seong reference utilizes a fixed amplitude generator rather than a fixed-frequency generator. Thus, elements 100, 200 and 302 cannot show a frequency-fixed PWM signal generating circuit and the PWM output signal is not a second PWM signal having a fixed-frequency.

In general, the incoming signal Vo is compared to a reference signal in an error amplifier 301 to produce a second signal Vcon. Thus, this signal differs from the input signal by a set amount found in the reference signal. This signal is compared in 302 to a signal Vtr which is received from the sawtooth oscillating means 100. As mentioned at column 2, line 55 of the reference, a current is generated in the sawtooth controlling means 200, to control constantly the amplitude Δ V of the sawtooth voltage Vtr. Column 3, line 32 points out that comparator 302 modulates the width of the sawtooth voltage Vtr. Column 4, lines 6-11 specifically points out that the amplitudes of the sawtooth voltage Vtr are always constantly maintained and that the output of comparator 302 is a pulse modulating signal which remains stable. Applicants have reviewed the entire reference and see no indication that the output signal has fixed-frequency or that the circuitry referred to by the Examiner is a frequency-fixed signal generating circuit.

The present invention is used to fix the frequency of the output PWM signal (paragraph 0003) to provide a relatively high frequency at which to operate the fan motor in order to avoid noise. The buffer circuit 20 includes a frequency-fixed PWM signal generating circuit in order to generate a second PWM signal having a fixed frequency. However, this is not taught in Seong which only teaches the maintenance of a voltage amplitude Δ V or to reach system optimization as shown in Figures 4A to 4C. Thus, it is clear that Seong has a fixed amplitude system rather than a fixed frequency system.

Accordingly, Applicants submit that claim 1 is not anticipated by this reference since the reference does not show a frequency fixed PWM signal generating circuit and does not show a second PWM signal having a fixed frequency as required by the second paragraph of claim 1.

Dependent Claims 4, 7 and 9

Claims 4, 7 and 9 depend from claim 1 and are allowable based on the allowability of that independent claim. In addition, claim 4 describes a frequency controller and a PWM signal generator. The Examiner has equated these two elements to a combination of circuits 100 and 200 and circuit 302. Applicants submit that the reference does not show a frequency controller which determines the fixed frequency of the second PWM signal. This is for the same reason recited above that the second PWM signal does not have a fixed frequency.

In regard to claim 9, the Examiner only indicates that Seong implicitly teaches all duty cycle ranges since there is no limit. Applicants submit that this Examiner has not met his burden of proof showing that these features are found in the reference.

Rejection of Claims 3 and 20 Under 35 U.S.C. 103(a) as Being Unpatentable Over Seong

Claim 3 specifically relates to the embodiment shown in Figure 6 which uses the implementation of a microchip control unit except through software programs. Claim 20 is the equivalent of a combination of claims 1 and 3.

Dependent Claim 3

The Examiner refers to column 4, lines 15-18 to teach the features of claim 3. However, this section only indicates that the Seong invention can be used in an integrated circuit to control the switching mode power supply. Applicants submit that this does not teach the implementation by a microchip control unit set through software programs. The Examiner indicates that it would be obvious to incorporate software programs for either automation or selecting purposes. Applicants submit the Examiner has not pointed out why such an implementation would be obvious to one skilled in the art. Furthermore, Applicants submit that this meager teaching at the very end of the specification of Seong does not teach us such a possibility. Accordingly, Applicants submit that claim 3 is not obvious over this reference.

Independent Claim 20

Independent claim 20 includes the limitations of claims 1 and claim 3. Accordingly, Applicants submit that claim 20 is allowable for the reasons recited above in regard to claim 1 and also for the reasons recited in regard to claim 3.

Rejection of Claims 6, 10, 11, 13, 14, 16, 17, 19 and 21 Under 35 U.S.C. 103(a) as Being Obvious Over Seong in view of Hoffman (US Patent 5,457,435)

In this rejection, the Examiner relies on the Hoffman reference to teach the use of a resistor 230 coupled to the output of an operational amplifier 224 to provide the output signal.

Claim 6

Claim 6 depends from claim 4 and is allowable for the reasons recited above in regard to that claim. In addition, claim 6 recites the resistor connected to an output terminal of the operational amplifier. Applicants submit that even if Hoffman does teach such a resistor coupled to the output of the operational amplifier, that this claim remains allowable based on its dependency.

Independent Claim 10

Claim 10 relates to the control circuit for the speed of a fan motor including a signal generation circuit, shown as number 10 in Figure 2, a PWM buffer circuit shown as number 20 in Figure 2, and a driving circuit shown as number 11 in Figure 2 to control the speed of a fan motor 12 shown in Figure 2. The Examiner has not specifically pointed out a circuitry which corresponds to the signal generation unit, the driving circuit and the fan motor. The Examiner has referred to claim 6, and inferentially to claim 1 which does relate to the buffer circuit. The Examiner has only mentioned that load 112 is the equivalent of the driving circuit and fan motor and that the limitation of controlling the speed of the fan motor is an intended use. It is noted that the Examiner has not indicated where the PWM signal generation unit is found. Applicants

also note that the Examiner has not referred to the prior art Figure 1 of the present application either. Applicants submit that the Examiner has not met the limitations of claim 10.

Claim 11

Claim 11 has similar limitations to claim 1 and depends from claim 10. Claim 11 is allowable for the reasons recited above in regard to claim 10 and is also allowable for the reasons recited above in regard to claim 1.

Dependent Claims

Dependent claims 13, 14, 16, 17 and 19 depend from claim 10 and are allowable for the same reasons recited above. In addition, these claims also contain similar recitations to claims 3, 4, 6, 7 and 9 and are similarly allowable for the reasons presented there.

Independent Claim 21

Independent claim 21 is a combination of limitations found in 10, 11 and 13. Applicants submit that this claim is likewise allowable for all of the reasons presented in regard to these three claims.

VIII. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE

No evidence pursuant to sections 1.130, 1.131 or 1.132 are entered by or relied upon by the Examiner as being submitted.

X. RELATED PROCEEDINGS

There are no related proceedings.

Dated: November 3, 2006

Respectfully submitted,

By _____ ROBERT F. GNUSE
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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/657,181

1. A pulse width modulation (PWM) buffer circuit comprising:

a duty cycle converting circuit for receiving a first PWM signal and then generating a duty cycle reference voltage based on a first duty cycle of the first PWM signal, wherein the duty cycle reference voltage is a one-to-one mapping function of the first duty cycle; and

a frequency-fixed PWM signal generating circuit, coupled to the duty cycle converting circuit, for receiving the duty cycle reference voltage and then outputting a second PWM signal having a fixed frequency, wherein the second PWM signal has a second duty cycle determined on the basis of the duty cycle reference voltage, and the second duty cycle is a one-to-one mapping function of the duty cycle reference voltage.

2. The PWM buffer circuit according to claim 1, wherein the duty cycle converting circuit comprises:

a transistor having a gate for receiving the first PWM signal and a source coupled to ground;

a first resistor connected between a drain of the transistor and a voltage source;

a diode having a P electrode connected to the drain of the transistor;

a second resistor connected between an N electrode of the diode and the ground;

a first capacitor connected between the N electrode of the diode and the ground;

a first operational amplifier having a non-inverting input terminal connected to the N

electrode of the diode;

a third resistor connected between an inverting input terminal of the first operational amplifier and the ground;

a fourth resistor connected between the inverting input terminal of the first operational amplifier and an output terminal of the first operational amplifier; and

a fifth resistor connected between the output terminal of the first operational amplifier and the frequency-fixed PWM signal generating circuit.

3. The PWM buffer circuit according to claim 1, wherein the frequency-fixed PWM signal generating circuit is implemented by a microchip control unit set through software programs.

4. The PWM buffer circuit according to claim 1, wherein the frequency-fixed PWM signal generating circuit comprises:

a frequency controller for providing a frequency control signal to determine the fixed frequency of the second PWM signal, and

a PWM signal generator, coupled to the duty cycle converting circuit and the frequency controller, for generating the second PWM signal in response to the duty cycle reference voltage and the frequency control signal.

5. The PWM buffer circuit according to claim 4, wherein the frequency controller comprises:

an operational amplifier having a non-inverting input terminal, an inverting input terminal, and an output terminal;

a first resistor connected between the non-inverting input terminal of the operational amplifier and the ground;

a second resistor connected between the non-inverting input terminal of the operational amplifier and the output terminal of the operational amplifier;

a capacitor connected between the inverting input terminal of the operational amplifier and the ground; and

a third resistor connected between the non-inverting input terminal of the operational amplifier and the output terminal of the operational amplifier.

6. The PWM buffer circuit according to claim 4, wherein the PWM signal generator comprises:

an operational amplifier having a non-inverting input terminal connected to the duty cycle converting circuit for receiving the duty cycle reference voltage and an inverting terminal connected to the frequency controller for receiving the frequency control signal, and

a resistor having a terminal connected to an output terminal of the operational amplifier such that the second PWM signal is output through another terminal of the resistor.

7. The PWM buffer circuit according to claim 4, wherein the frequency control signal is a continuous triangular wave signal.

9. The PWM buffer circuit according to claim 1, wherein the fixed frequency of the second PWM signal is higher than 10 kHz and a frequency of the first PWM signal is higher than 30 Hz and the first duty cycle is ranged from5% and 95%.

10. A control circuit for speed of a fan motor, comprising:

a PWM signal generation unit for generating a first PWM signal having a first duty cycle;

a PWM buffer circuit, coupled to the PWM signal generation unit, for converting the first PWM signal into a second PWM signal having a fixed frequency and a second duty cycle; and

a driving circuit, coupled to the PWM buffer circuit, for outputting a driving signal based on the second PWM signal to the fan motor, thereby controlling the speed of the fan motor.

11. The control circuit according to claim 10, wherein the PWM buffer circuit comprises:

a duty cycle converting circuit for receiving the first PWM signal and then generating a duty cycle reference voltage based on the first duty cycle of the first PWM signal, wherein the duty cycle reference voltage is a one-to-one mapping function of the first duty cycle, and

a frequency-fixed PWM signal generating circuit, coupled to the duty cycle converting circuit, for receiving the duty cycle reference voltage and then outputting the second PWM signal, wherein the second duty cycle of the second PWM signal is determined on the basis of the duty cycle reference voltage, and the second duty cycle is a one-to-one mapping function of the duty cycle reference voltage.

12. The control circuit according to claim 10, wherein the duty cycle converting circuit comprises:

a transistor having a gate for receiving the first PWM signal and a source coupled to ground;

a first resistor connected between a drain of the transistor and a voltage source;

a diode having a P electrode connected to the drain of the transistor;

a second resistor connected between an N electrode of the diode and the ground;

a first capacitor connected between the N electrode of the diode and the ground;

a first operational amplifier having a non-inverting input terminal connected to the N electrode of the diode;

a third resistor connected between an inverting input terminal of the first operational amplifier and the ground;

a fourth resistor connected between the inverting input terminal of the first operational amplifier and an output terminal of the first operational amplifier; and

a fifth resistor connected between the output terminal of the first operational amplifier and the frequency-fixed PWM signal generating circuit.

13. The control circuit according to claim 10, wherein the frequency-fixed PWM signal generating circuit is implemented by a microchip control unit set through software programs.

14. The control circuit according to claim 10, wherein the frequency-fixed PWM signal generating circuit comprises:

a frequency controller for providing a frequency control signal to determine the fixed frequency of the second PWM signal, and

a PWM signal generator, coupled to the duty cycle converting circuit and the frequency controller, for generating the second PWM signal in response to the duty cycle reference voltage and the frequency control signal.

15. The control circuit according to claim 14, wherein the frequency controller comprises:

a operational amplifier having a non-inverting input terminal, an inverting input terminal, and an output terminal;

a first resistor connected between the non-inverting input terminal of the operational amplifier and the ground;

a second resistor connected between the non-inverting input terminal of the operational amplifier and the output terminal of the operational amplifier;

a capacitor connected between the inverting input terminal of the operational amplifier and the ground; and

an third resistor connected between the non-inverting input terminal of the operational amplifier and the output terminal of the operational amplifier.

16. The control circuit according to claim 14, wherein the PWM signal generator comprises:

an operational amplifier having a non-inverting input terminal connected to the duty

cycle converting circuit for receiving the duty cycle reference voltage and an inverting terminal connected to the frequency controller for receiving the frequency control signal, and

a resistor having a terminal connected to an output terminal of the operational amplifier such that the second PWM signal is output through another terminal of the resistor.

17. The control circuit according to claim 14, wherein the frequency control signal is a continuous triangular wave signal.

19. The control circuit according to claim 10, wherein the fixed frequency of the second PWM signal is higher than 10 kHz and a frequency of the first PWM signal is higher than 30 Hz and the first duty cycle is ranged from 5% and 95%.

20. A pulse width modulation (PWM) buffer circuit comprising:

a duty cycle converting circuit for receiving a first PWM signal and then generating a duty cycle reference voltage based on a first duty cycle of the first PWM signal, wherein the duty cycle reference voltage is a one-to-one mapping function of the first duty cycle, and

a frequency-fixed PWM signal generating circuit, coupled to the duty cycle converting circuit, for receiving the duty cycle reference voltage and then outputting a second PWM signal having a fixed frequency, wherein the second PWM signal has a second duty cycle determined on the basis of the duty cycle reference voltage, and the second duty cycle is a one-to-one mapping function of the duty cycle reference voltage, and the frequency-fixed PWM signal generating circuit is implemented by a microchip control unit set through software programs..

21. A control circuit for speed of a fan motor, comprising:

a PWM signal generation unit for generating a first PWM signal having a first duty cycle;

a PWM buffer circuit, coupled to the PWM signal generation unit, for converting the first PWM signal into a second PWM signal having a fixed frequency and a second duty cycle, wherein the PWM buffer circuit comprises:

a duty cycle converting circuit for receiving the first PWM signal and then generating a duty cycle reference voltage based on the first duty cycle of the first PWM signal, wherein the duty cycle reference voltage is a one-to-one mapping function of the first duty cycle, and

a frequency-fixed PWM signal generating circuit, coupled to the duty cycle converting circuit, for receiving the duty cycle reference voltage and then outputting the second PWM signal, wherein the second duty cycle of the second PWM signal is determined on the basis of the duty cycle reference voltage, and the second duty cycle is a one-to-one mapping function of the duty cycle reference voltage and the frequency-fixed PWM signal generating circuit is implemented by a microchip control unit set through software programs; and

a driving circuit, coupled to the PWM buffer circuit, for outputting a driving signal based on the second PWM signal to the fan motor, thereby controlling the speed of the fan motor.